

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Harari, Eliyahou; Mehrotra, Sanjay; Norman, Robert

Assignee:

Title: Flash EEPROM System

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Group Art Unit: 2818

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San Francisco, California

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BOX NON-FEE Amendment
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE TO OFFICE ACTION

Dear Sir: These remarks are in response to the Office Action mailed on mailed on April 2, 2001, setting a response period expiring on July 2, 2001, and for which a one month extension is hereby requested. The Office Action objected to the drawings, requested a substitute specification, and rejected all of the pending claims 35 U.S.C. 112, first paragraph. These are all dealt with under the appropriate heading below.

Objections to the Drawings

The various elements listed in the objection to the drawings are the same as those recited under the rejection of the claims under 35 U.S.C. 112, first paragraph. It is respectfully submitted that all of the claimed features are included in the drawings. The appropriate drawings and the various elements are cited below in the response to the 35 U.S.C. 112 rejection.

Substitute Specification

A substitute specification was filed together with the present application and preliminary amendment. For the Examiner's convenient, another copy as well as a marked copy has been included with the present Response.

LAW OFFICES OF
SKJERNEN MORRILL
MACPHERSON LLP
HREE EMBARCADERO CENTER
28th FLOOR
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

Rejections under 35 U.S.C. 112, first paragraph

The Office Action rejected claims 63-72 under 35 U.S.C. 112, first paragraph, as not containing a number of limitations found in the claims. This rejection is respectively submitted to be in error. Much of the support for these claims is contained in the material contained in the Preliminary Amendment and in U.S. Patent Number 5,095,344 (formerly application Serial Number 204,175 and referred to as the '344 patent below) that is incorporated in the present application in several places, such as page 11, lines 25-31 (page 12, lines 15-21 of the Substitute Specification).

Concerning the first and second groups of non-volatile memory cells coupled in parallel between a bit-line and a reference potential, see, for example, Figure 12 of the present application or Figures 15a and 15b of the '344 patent.

A plurality of sense circuits including at least a first, a second and a third sense circuit are shown in Figure 11e of the '344 patent. The various steps of operating the memory device are described in the '344 patent, for example, from column 23, line 25, to column 27, line 3. In particular, the reference parameters I_{REF} are shown in Figure 11c of the '344 patent (that is also Figure 15B of the additional figures of the present application), with the parallel read operation is shown in the lower right hand portion of Figure 11e of that patent.

The relationship among the various threshold ranges as recited in claim 73 are shown in Figure 15A of additional figures of the present application. The column select circuit and other structure of claim 75 is shown, for example, in Figure 12 of the present application. The sense circuit of claim 76 is again shown in the lower right hand portion of Figure 11e of the '344 patent.

Therefore it is respectfully submitted that the rejections of claims 63-72 are not well founded and that they are allowable for the reasons given above. As noted in the Preliminary Amendment filed with present application, these claims are substantial copies of claims 1, 3-4, 6, 13, 15-17, 19-20, and 29-33, respectively, of U.S. Patent number 6,014,327 of Banks. A Request for a Declaration of Interference with this patent based upon these claims will be submitted shortly. ?

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Respectfully submitted,



Michael G. Cleveland
Attorney for Applicant(s)
Reg. No. 46,030

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
HREE EMBARCADERO CENTER
28th FLOOR
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646